RESEARCH DEPARTMENT

Digital coding equipment for recording field strength measurements

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DIGITAL CODING EQUIPMENT FOR RECORDING FIELD-STRENGTH MEASUREMENTS

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SUMMARY

This report describes a voltage coder and tape perforator which samples the d.c. output from one or more field-strength recording receivers at regular intervals and records the values by means of a 5-unit binary code, on a paper tape which can subsequently be fed into a computer for analysis.

1. GENERAL

The coder is an improved version of an eight-channel voltage coder described in an earlier report[1] and is intended to be used initially for propagation tests in conjunction with u.h.f. recording receivers[2]. Any number of receivers from one to eleven may be connected to the coder which will sample each one in turn. Interchangeable cams give sampling rates of 1, 2 or 3 readings per minute. The 0 to -3V input from the receivers is coded in thirty steps of 100 mV each (thirty-one levels). The thirty-second character of the five digit binary code, the 'all-blank', is used as an identification of the start of the sampling cycle of a group of receivers.

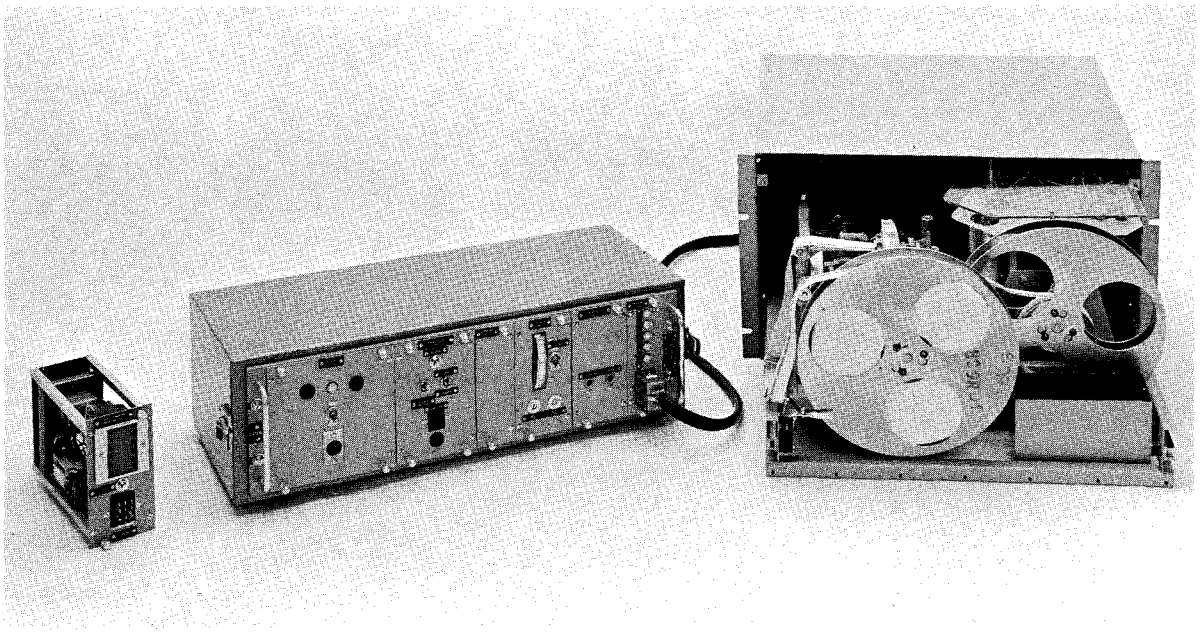
A prototype equipment has been in use for more than a year and has given good agreement between automatic and hand analysis[3].

Although the coder was designed primarily for use with field strength measuring receivers, it can be adapted for coding any variant which can be made to have a range of 0 to -3V; for example a similar equipment is being used to record variations in the frequency of the mains supply[4].

A photograph of a coder and a tape perforator is shown in Fig. 1.

2. DESCRIPTION OF APPARATUS

A block schematic diagram of the complete apparatus is given in Fig. 2. The coder consists of six sub-units which plug into a 19 inch (483 mm) bay mounting frame carrying the interconnecting cables. The input unit is made in two versions, one a single channel unit for use when the output of only one receiver is being



(a) *(b)* *(c)*

Fig. 1 - Photograph of coder and tape perforator

(a) Multi-channel input unit *(b)* Coder with single channel input unit
(c) Tape perforator

recorded and the other a multi-channel unit which permits the outputs of up to eleven receivers to be recorded on one tape.

The main function of the equipment is to transform the input voltage (0 to -3V) into five-digit binary form. This means that the five control outputs representing values in 100 mV units of 16, 8, 4, 2 and 1 must be formed, each output being in either the 'on' or 'off' state.

The transformation is achieved with a reversible binary counter by steering the counter to the correct value in the following way. The total value that corresponds to the state of the counter at any moment is formed as a voltage by a reconstitution circuit. This adds currents corresponding to the binary values 1 to 16 according to the state of each of the five stages of the counter to give the reconstituted voltage. This voltage is compared with the input voltage to produce an error signal which is chopped by an 800 c/s square wave. Thus the error voltage is converted into a square-wave whose amplitude indicates the magnitude of the error and whose phase relative to the chopping wave determines the sense of the error. This square-wave is amplified and applied (a) to a phase sensitive detector circuit for displaying the error on a d.c. meter, and (b) to a pulse forming network which, if the error signal exceeds a pre-set value, provides positive pulses for the counter unit.

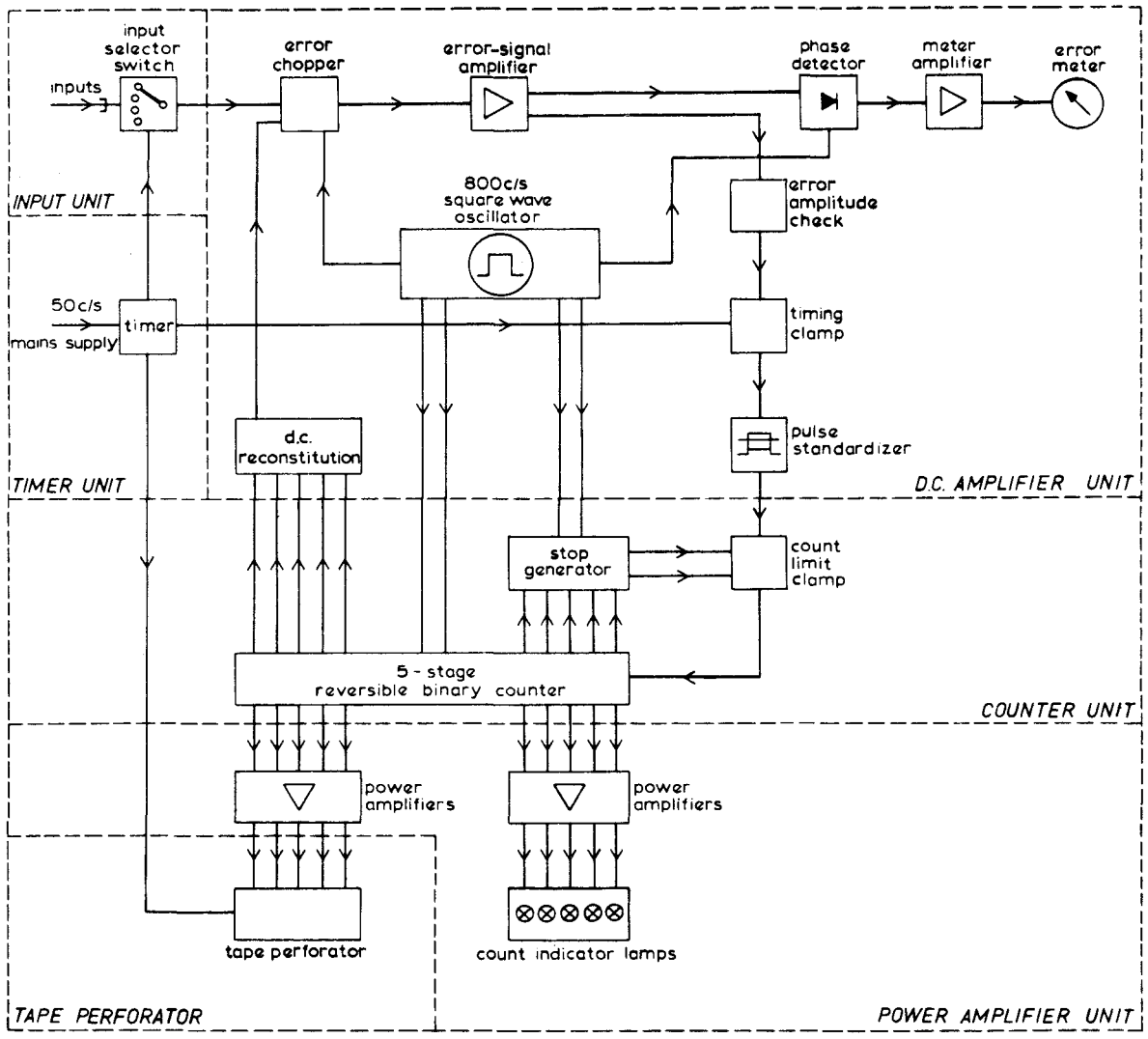


Fig. 2 - Block schematic

The positive pulses will occur in either the positive or negative half-cycle of the 800 c/s reference waveform, dependent on the sign of the error voltage. In operation the condition of the counter as to whether it counts upwards or downwards is reversed by alternate half-cycles of the reference waveform, so that any input pulse occurring during the positive phase will give an upward count while one occurring during the negative phase will give a downward count. In this manner the count and the reconstituted voltage follow the input voltage and, provided that the input variations are not too rapid, the error is kept to less than one step (100 mV). The 800 c/s switching is in fact sufficient to ensure that any slowly fading signal passed by the input filter can be followed by the counter.

After a period during which the counter follows the signal the count is temporarily frozen. This occurs at selected intervals of the order of one a minute, and the perforator solenoids are set to correspond to the count and holes punched in

the paper tape according to the binary code. The count conditions of zero and thirty are detected by the 'stop' generator which operates the count-limit clamp so as to prevent the counter from stepping further and giving false counts.

2.1. The Timing Unit

A simplified circuit diagram of the timing unit is given in Fig. 3. The sequence of operations within the coder is governed by the timing unit which contains two cam-operated microswitches actuated by a 1 r.p.m. synchronous motor. Interchangeable cams are provided to give either 1, 2 or 3 punches per minute. One of the switches operates the timing clamp and permits the signals to pass to the counters for half the total time, after which the clamp is released, the counter blocked, and the code solenoids set. Near the centre of the blocked period the other switch S2 closes and initiates the operation of the tape perforator and, when it is used, the stepping uniselector in the multi-channel input unit. Before S2 operates, a large capacitor C2 charges to -20V. The operation of the switch S2 connects this capacitor to the base of TR1 via R3 and so permits TR1 to conduct heavily. The output from TR1 drives the punch solenoid amplifier in the perforator unit. After approximately ¼ second the capacitor C2 will have discharged sufficiently to enable TR1 to cease conduction, thereby releasing the punch solenoid. The capacitor C2 continues to discharge through R4. When the switch S2 releases, the transistor TR2 is driven into conduction and C2 commences to charge. TR2 conducting drives the power amplifier TR3 into conduction and steps the uniselector in the multi-channel input unit. After approximately 50 ms C2 has recharged to -12V and TR2 will be cut-off. C2 continues to charge to -20V before the cycle is repeated.

A manual punch switch S5 is provided; this operates in a similar manner to S2 for the punch transistor TR1 but does not operate the stepping mechanism of the uniselector.

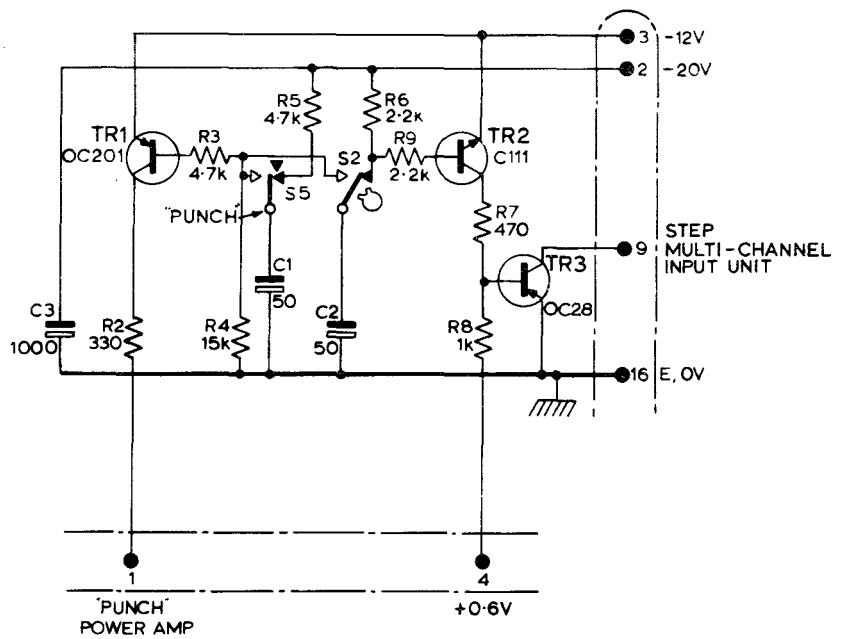


Fig. 3 - Timing unit

2.2. The Input Units

The input unit is made in two versions. When the output of only one receiver is being recorded the single-channel unit is used; this simply passes the input directly to the d.c. amplifier unit.

In the multi-channel unit, which permits inputs from up to eleven receivers to be recorded on the same tape, a uniselector selects each input in turn, and inserts an 'all-blank' into the code at the end of each sequence. If fewer inputs than eleven are required then inputs may be paralleled to increase the sampling rate and extra 'all-blanks' inserted as necessary. The extra 'all-blanks' are inserted by connecting the appropriate pins on an internal 12-pin plug.

The uniselector is also used to switch lamps to indicate which input is connected to the coder. A push button is provided to enable the uniselector to be operated manually.

2.3. The D.C. Amplifier Unit

A complete circuit diagram of the d.c. amplifier unit is given in Fig. 4.

The input to the unit passes through a simple low-pass filter R2, C2, to remove any residual hum or modulation on the signal. The input voltage and the output of the d.c. reconstitution circuit are clamped by TR1 for alternate half cycles of the 800 c/s square-wave oscillator TR14 and TR15. This clamping transistor is run in the inverted mode with the square-wave applied between its base and collector. Any square-wave produced by the alternate clamping and releasing action of TR1 is capacity coupled by C3 to the three-stage amplifier TR2 to TR4. The first and third stages of this amplifier have individual current feedback, and the second stage has voltage feedback, whilst d.c. feedback over the whole amplifier stabilizes the working potentials. The feedback of the third stage is adjusted by the 'trip level' control R21 which allows the overall gain to be preset.

One output from the amplifier is clamped to -12V by TR5 during the clamp phase of the square-wave oscillator. The low-pass filter R24, C11, feeds the resulting mean d.c. level from this clamp to one input of a long-tailed pair amplifier TR6, TR7. The other input of this pair is fed from a fixed potential preset by the 'SET ZERO' control. A resistor R70 between the emitters of this amplifier stabilizes the gain. A variable resistor R72 adjusts the balance of the collector loads and enables the temperature coefficient of the zero of the amplifier to be set accurately. A meter between the collectors of this amplifier indicates the error between the reconstituted voltage and the input.

The square-wave output from the amplifier TR2 to TR4 is also applied to the base of TR16 after d.c.-restoration by D3 so that it is negative with respect to earth potential. The latter transistor has a fixed potential of about -1½V on its emitter and will conduct only when the peak-to-peak value of the square-wave from the amplifier exceeds 1½V. The output from TR16 collector to the 'pulse standardizer' consisting of a Schmitt trigger pair TR18, TR19. As long as the error signal is sufficient this provides triggering pulses for the counter via the phase-reversing amplifier TR20. In order to block the counter before recording a sample, TR17 is

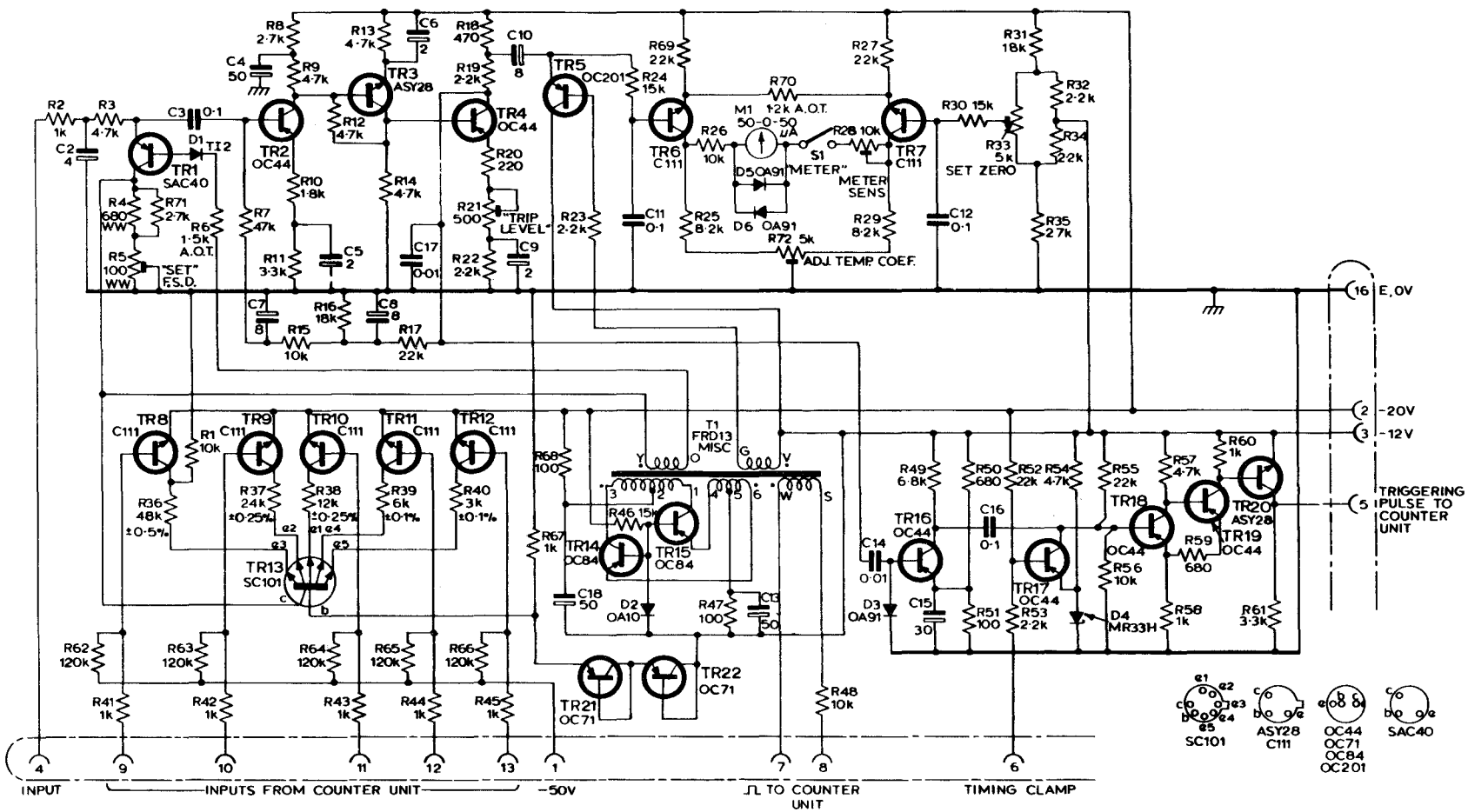


Fig. 4 - D.C. Amplifier unit

made heavily conducting by the appropriate timing signal and clamps the input to the Schmitt trigger at -3V, thus preventing TR18 from conducting.

The transistors TR8 to TR12 are connected one to each of the five binary counter outputs. These transistors will be either cut-off or heavily conducting. When conducting, their base-emitter potentials are less than 100 mV. One end of each collector load of these switching transistors is connected to one emitter of a five emitter transistor TR13. The base of this transistor is connected to a fixed potential of approximately -11½V. Since the five loads R36-R40 have resistance values in binary steps, the current passing will also be in binary steps. The collector current of TR13 is closely equal to the sum of its emitter currents but is independent of collector voltage, so that the voltage across the collector load R4, R5 will be proportional to the count in the binary counter. This voltage is the reconstituted voltage which is balanced against the input to the coder.

Some adjustment of the maximum value of the reconstituted voltage is given by the variable resistor R5 so that changes of up to ± ¼V in the input corresponding to the maximum count may be made. The change with temperature of base-to-emitter drop of TR13 and emitter-to-collector drop of TR8 to TR12 is compensated by the drop across transistors TR20 and TR21 connected to operate as low-impedance diodes.

2.4. The Counter Unit and Power Amplifier

The circuit diagram of the counter unit is given in Fig. 5. The counter consists of five similar stages of Eccles-Jordan binary pairs TR5, TR7, etc. and the diagram has been simplified by the omission of three stages. The input to the counter from the pulse standardizer is differentiated by C1, R114 and applied to the emitter of TR1. This transistor is normally just cut-off, but the pulse is sufficient to drive TR1 into conduction and so operate the counter. In order that the counter may be driven either forwards (increasing count) or backwards (decreasing count), as appropriate to reduce the error between the reconstituted voltage and the input to be coded, all four interstage couplings are modified every half-cycle of the reference 800 c/s switching signal. This function is performed by passing the 'carry one' count from one stage to the next via pairs of transistors such as TR6, TR8 shown for the first stage in Fig. 5. One member of the pair is held just cut-off and the other well beyond cut-off by the 800 c/s square-wave; their conditions are therefore reversed each half-cycle. A trigger pulse is passed on only through the transistor that is just cut-off and, since the transistors are connected to opposite sides of the binary stage, the count is passed on for a 0 to 1 transition for the first half-cycle and for a 1 to 0 transition for the second half-cycle. This means the direction of count is in the reverse direction for alternate half-cycles as required by the principle of operation already explained. The output winding of the 800 c/s oscillator is floating but D20 and D23 are used to self-bias this square-wave to the correct potential, thus eliminating the effect of any changes in amplitude of the oscillation.

When the counter has reached either a maximum or minimum count, further changes in the same direction must be prevented or an indeterminate count would be obtained. These limiting counts are detected by the diodes D19, D24 etc. and when the limit is reached and the square-wave, as detected by D2, D7, is in the appropriate direction, either TR2 or TR3 will conduct. This will take TR1 well beyond cut-off and prevent any further count in the same direction.

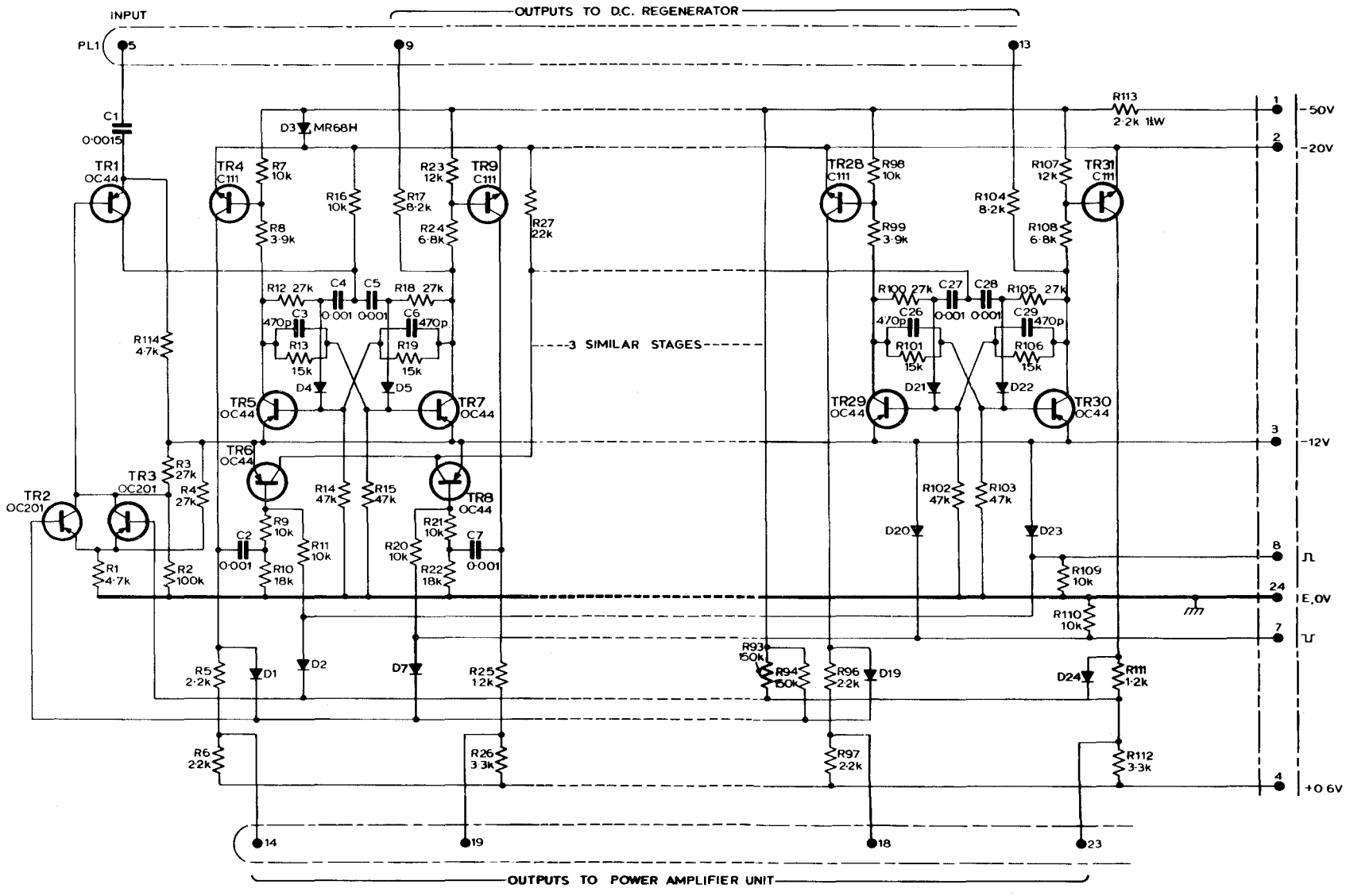


Fig. 5 - Counter unit

Each of the counter stages has three outputs to other units. The first drives the d.c. reconstitution circuit via R17 etc., while the other two have output amplifiers TR4, TR9 etc. These outputs drive power amplifiers for operating the code solenoids in the perforator unit and indicator lamps to show the state of the count.

The power supplies to the amplifiers operating the code solenoids are gated so that the solenoids are not operated during the time that the counters are running, thus preventing undue wear.

A conventional power supply unit provides an unstabilized output of -50V and stabilized outputs of -20V, -12V and +0·6V. A protective device cuts off the power supply in the event of a severe overload.

3. THE TAPE PERFORATOR UNIT

This unit contains a modified commercial tape perforator together with power supplies and a spooling motor. The principal modifications to the perforator are a new chad shute and the substitution of a d.c. operated rotary solenoid for the a.c. solenoid. The unit, a simplified circuit of which is shown in Fig. 6, contains a three-stage transistor amplifier to operate the punch solenoid. The first transistor TR1 is normally conducting heavily but is cut-off by an incoming punch pulse. The low collector potential of TR1 together with the 0·6V drop across the diode D2 maintains TR2 and TR3 cut-off except during the punch pulse when these transistors will conduct. The transistors TR2 and TR3 are connected as a grounded emitter 'Darlington pair'[5] and on conduction will pass a large (4A) current through the solenoid. The power supply is a simple bridge rectifier circuit giving about 25V off load. This voltage falls to about half during the punch pulse. The code solenoids are directly connected to the coder outputs.

In order to 'run through' paper tape, twin push-buttons are provided. One of these switches removes the supplies from the code solenoids and the other, S2, connects a discharged capacitor C1 across the base of TR1, causing the punch solenoid

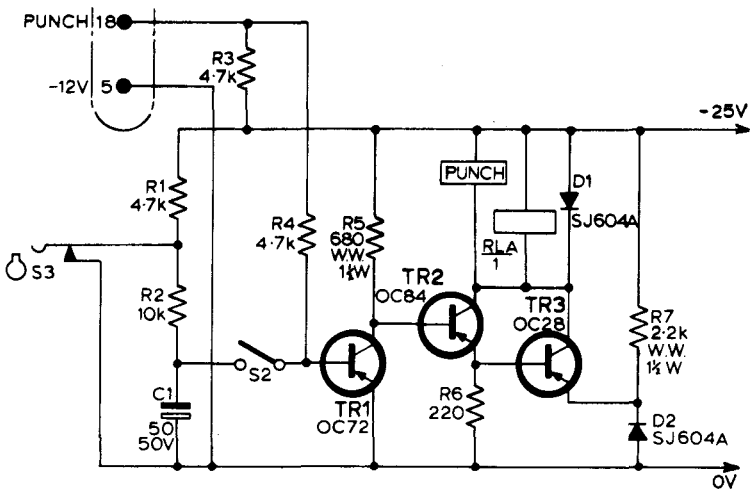


Fig. 6 - Tape perforator unit

to operate. During the punch operation the cam-driven switch S3 operates and allows C1 to charge, thereby releasing the punch. This process is repeated continuously whilst the buttons are depressed.

The mains-operated tape-winder has its power supplies connected by relay A during the punch pulse only. This relay is wired in parallel with the punch solenoid.

4. PERFORMANCE

The coder translates into binary form a 0 to -3V input giving thirty steps of 100 mV. The centre point of these steps is within ± 2 mV of the correct value and will not change by more than ± 2 mV over a temperature range of -10°C to +45°C. The stepping rate of the counter is 800 steps per second, giving a maximum balance time of less than 40 ms. The following rate on a varying input is limited by the low-pass filter on the input to a few cycles per second, dependent on the source impedance.

5. REFERENCES

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